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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,597	01/15/2002	Shunpei Yamazaki	07977-290001/US5432	4657

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,597	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24-30,32-38 and 40-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-22,24-30,32-38 and 40-64* is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,65,66 and 68* is/are rejected.

7)☒ Claim(s) *3,7 and 67* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action is in response to Amdt. A, filed 9/10/03

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,118,506 to Yamazaki et al.

Yamazaki discloses a light emitting device comprising: a thin film transistor (307-312) over a substrate (301); an interlayer insulating film (313,315) over the TFT; and a capacitor storage (319) over the insulating film (figure 4B), wherein the capacitor storage has a connection wiring line (318), a capacitance wiring line (316), and an insulating film (317) formed between the wiring lines (figures 4A, 4B), wherein the connection wiring line is connected to a source or drain of the TFT (figure 4B), and wherein the connection wiring line overlaps an active layer of the TFT (figure 4B).

3. Claims 1, 4, 5, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,747,830 to Okita.

Regarding claims 1 and 5, Okita discloses a light emitting device comprising: a TFT (5-9) over a substrate (1); an interlayer insulating film (12) over the TFT; and a capacitor storage

(14-16; column 6, lines 7-12) over the interlayer insulating film (figure 1), wherein the capacitor storage has a connection wiring line (16), a capacitance wiring line (14), and an insulating film (15) between the two, wherein the connection wiring line is connected to a source or drain of the TFT (figure 1) and overlaps the active layer of the TFT (figure 1).

Regarding claims 4 and 8, Okita discloses that the device includes notebook and mobile computers (column 5, lines 20-26).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 65 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,521,913 to Murade in view of Okita.

Regarding claim 65, Murade discloses a light emitting device comprising a plurality of pixels (figure 1, all pixels along row G1) each having a TFT (30) and a capacitor storage (70), wherein all of the capacitor storages of the plurality of pixels share one capacitance wiring line (3b, figure 1), wherein each of the capacitor storages of the plurality of pixels has a connection wiring line (80), and an insulating film (81) between the connection and capacitance wiring lines (figures 1-3), wherein the connection wiring line is connected to a drain region (1c) of the TFT, and wherein the capacitance wiring line overlaps an active layer of the TFT of each of the plurality of pixels (figures 8 and 12).

Murade fails to disclose that the capacitance wiring line is formed on a different layer from a gate electrode of the TFT.

Okita teaches that it's advantageous to provide a storage capacitance above the TFT, and thus having a capacitance wiring line above the layer of the gate electrode, in order to maximize the pixel display area (column 7, line 55 – column 8, line 3; figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display structure of Murade, such that the capacitance wiring line is formed above the layer of the gate electrode of the TFT, as taught by Okita. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide the capacitor entirely above the TFT, because doing so increases the size of the pixel display area, which allows the display to have a high opening ratio and a bright image (Okita, column 7, lines 55-67).

Regarding claim 68, Murade discloses that the appliance is a notebook personal computer or a mobile computer (column 36, lines 26-40).

6. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okita in view of U.S. Patent No. 6,121,652 to Suzawa (cited by applicant).

Okita fails to disclose that the insulating films are formed by anodization.

Suzawa discloses that the insulating films (layer above 417) between the storage capacitor lines can be formed by anodization (column 2, lines 52-58; column 8, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating film of Okita, so that it is an anodic oxide, as taught by

Suzawa. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an anodic oxide, because doing so simplifies the fabrication procedure, by eliminating the need for depositing a separate dielectric layer.

7. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murade in view of Okita as applied to claim 65 above, and further in view of Suzawa.

Murade fails to disclose that the insulating films are formed by anodization.

Suzawa discloses that the insulating films (layer above 417) between the capacitive plates can be formed by anodization (column 2, lines 52-58; column 8, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating film of Murade as modified by Okita, so that it is an anodic oxide, as taught by Suzawa. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an anodic oxide, because doing so simplifies the fabrication procedure, by eliminating the need for depositing a separate dielectric layer.

Allowable Subject Matter

8. Claims 9-22, 24-30, 32-38, and 40-64 are allowed.

9. Claims 3, 7, and 67 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to teach pixel features, such as forming a capacitive wiring line and a pixel electrode from the same film, providing a capacitive storage above switching and driving TFTs in an OLED structure, providing multiple vertically stacked capacitive storages in an OLED structure, or providing two completely distinct storage capacitors in an OLED structure. The primary reason for allowance is that although some related features, such as the advantages to placing a single storage capacitor above a TFT of a LCD pixel, are generally known in the art, there is no suggestion in the art to arrange the components of an OLED pixel in the manner claimed. It is the examiner's opinion that any significant structural or geometric changes to an OLED device significantly change the complexity of the fabrication process, the amount of interference between various signal lines, and the tendency of various components to block light emission, and thus, the claimed structural changes are considered critical and unobvious differences over the prior art.

11. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

12. Applicant's arguments with respect to claims 1, 5, and 65 have been considered but are moot in view of the new grounds of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

14. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233, until 2/9/04, and will be (571) 272-1690 after 2/9/04. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

ERIK J. KIELIN
PRIMARY EXAMINER